EMC Event Sept 2018

PCB Layout for EMC –
Common Pitfalls and Some Tips

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ESDI

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- *Use in any particular design is the responsibility of the designer and ESDI cannot guarantee accuracy and assumes no risk or liability whatsoever for its use.*

Electronic & Software Design, Inc.

- John Severson, PE – 30 years designing electronic systems and PC boards
- PCBs with high speed logic, precision mixed signal, wireless, video, CCD/digital imaging, graphics, LCD display monitor controllers
- Embedded Microcontrollers and Linux Software
- Design for EMC, RF Modules integration, RFID systems
- SolidWorks (3D) and Altium Designer

PCB layout for EMC – Common Pitfalls – and Some Tips

- PCB Layout for EMC is a large and complex topic.
- The focus of this presentation is Radiated EMI – RF coming from the PCB and attached cables -- 30 MHz to 1 GHz (and above)
- Based on my experience in making our designs able to pass at the test lab and helping others to do the same. -- from a Designer's Perspective

Outline

- Brief 5 minute review of some EMI concepts
- Some key sources of radiated EMI from PCBs
- Some common layout pitfalls
- A few tips for simplifying debug and test
- Questions

Brief Review of EMI Concepts

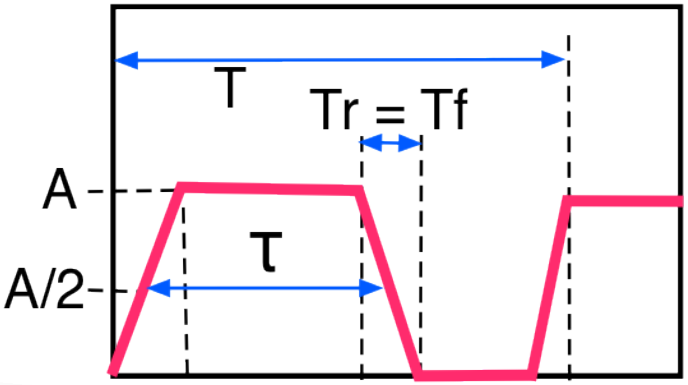
- Frequency, Wavelength, and the Time Domain
- Differential vs. Common Mode
- Coupling Mechanisms
- EMI vs. Loop Area
- RF Impedance
- Ground Planes

Frequency, Wavelength, and the Time Domain

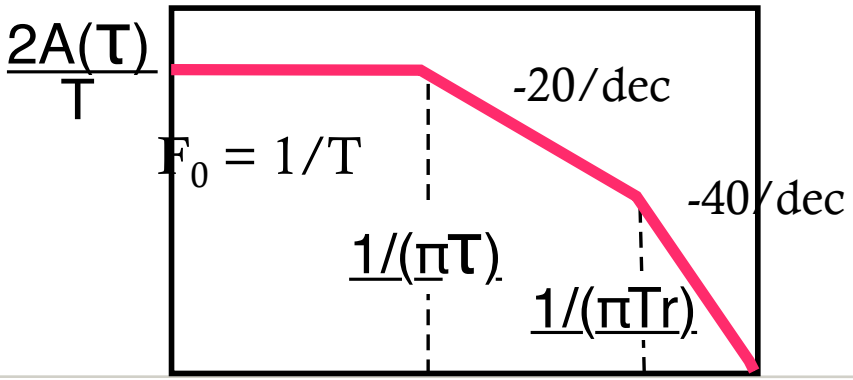
- $\lambda = 300/f_{(MHz)}$ in meters (in air)
- Electrically "small" features < $\lambda/20$
  - 6" at 100MHz ; 2" at 300MHz
- Consider the design at DC – 1MHz – 100MHz etc.

λ is less in PCB ~ $\frac{1}{\sqrt{\varepsilon_r}}$

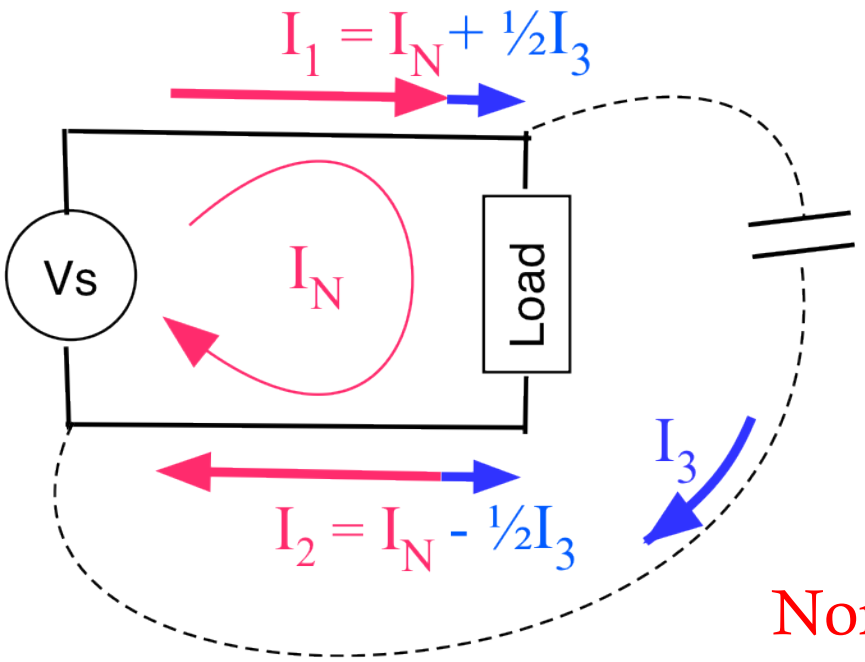
Digital Signal Time domain



Frequency domain (bounds)



Differential (Normal) and Common Mode



An unbalance (e.g., stray capacitance) can introduce a common mode current

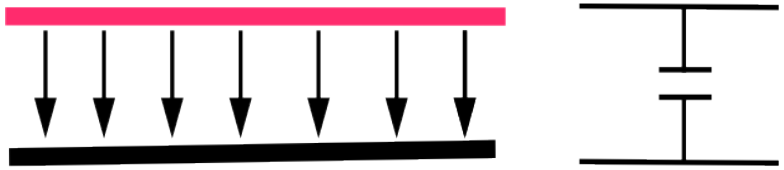
Normal Mode = I_N

Common Mode = $I_{CM} = \frac{1}{2}I_3$

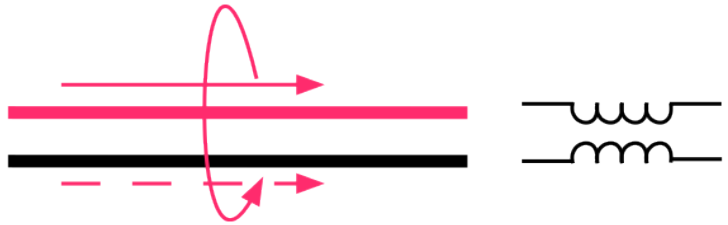
I_{CM} reduces signal integrity and causes EMI

Coupling Mechanisms

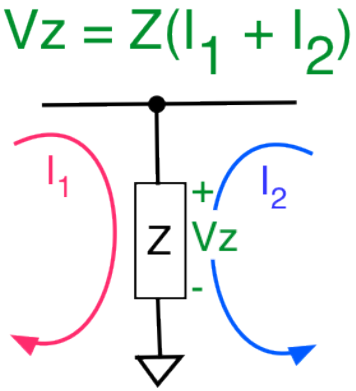
- Capacitive (Electric Field)



- Inductive (Magnetic Field)



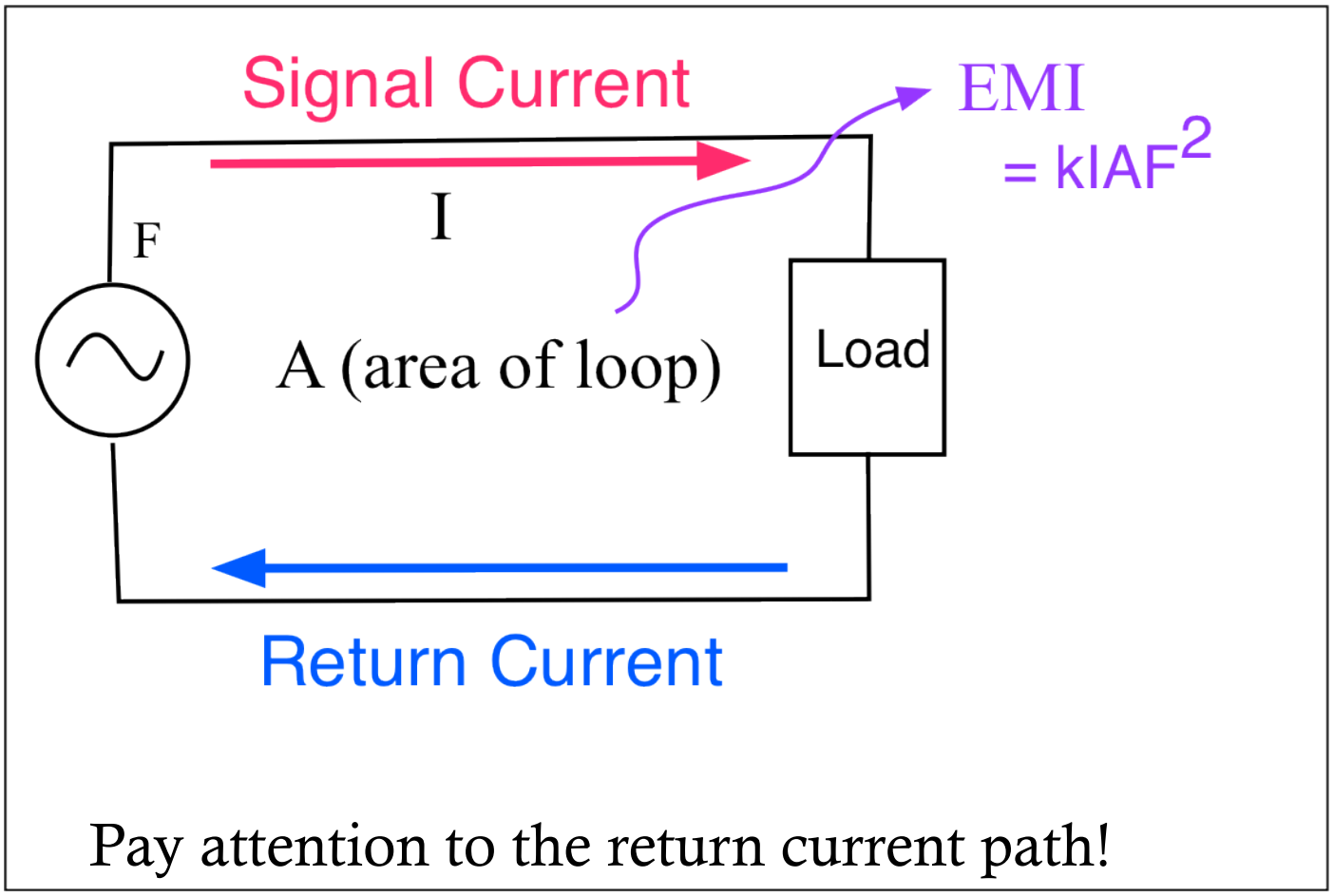
- Common (Shared) Impedance



RF Impedance

- **Z = R + jX**;
  - At DC to a few kHz, R dominates
  - At RF frequencies, X dominates
- Real components aren't ideal
- Paths and Proximity often dominate over components' characteristics
- At RF, the "skin effect" constrains the current flow to the outer surface of a conductor.

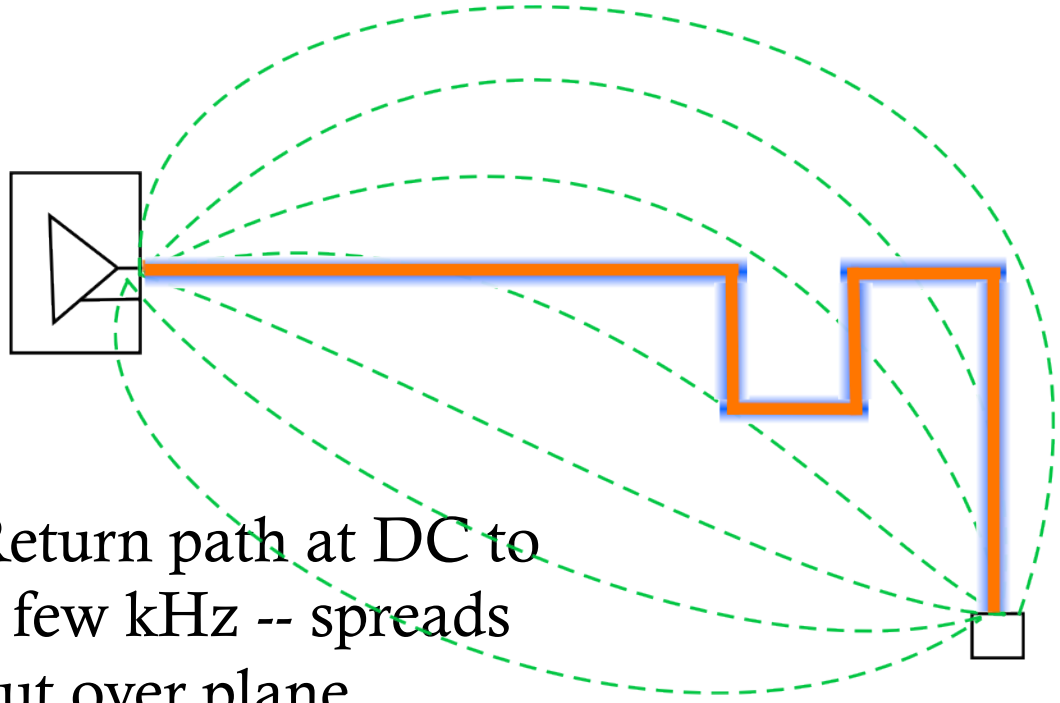
Minimize the loop area



Pay attention to the return current path!

Ground Plane Return Current Path

- The return path depends strongly on frequency:



Return path at DC to a few kHz -- spreads out over plane

Return path at MHz -- Closely follows signal trace

Key PCB EMI Sources

- Common Mode PCB Noise Gets onto Cables
- Return Current Discontinuities
- Large Current Loops Areas
- High Ground Impedance (at RF)
- Resonances

Fast rise time, high duty cycle signals are the most problematic, *and can couple to other signals*!

6 Common Layout Pitfalls…

1. **Not Starting EMI Planning and Design Up Front**

1. Start EMI Planning and Design Up Front – Have a Plan

- What are the applicable regulatory requirements and system specs?
- Identify all IO (including power) – and plan on how to handle them.
- Shielded or unshielded enclosure?
- Off the shelf (e.g. FCC or CE "pre-approved") often can be problematic.
- Many other considerations

Some Typical Board Planning Steps

- Identify high speed circuitry and group in zones to keep high speed lines short and to a minimum
- Plan to filter signals entering and leaving zones
- Mixed signal and switching supplies require special consideration
- Try to keep IO connectors together near a good ground (and the shield opening).
- Don't place High Speed Circuitry between IO connectors

Remember: Safety and Function First

- **Make sure EMI countermeasures…**
- **Don't compromise electrical safety requirements** such as grounding, isolation, creepage and clearance requirements, etc.
- **Preserve** the "in-band" **signal integrity** (such as analog noise, bandwidth, high speed digital signaling, etc.).

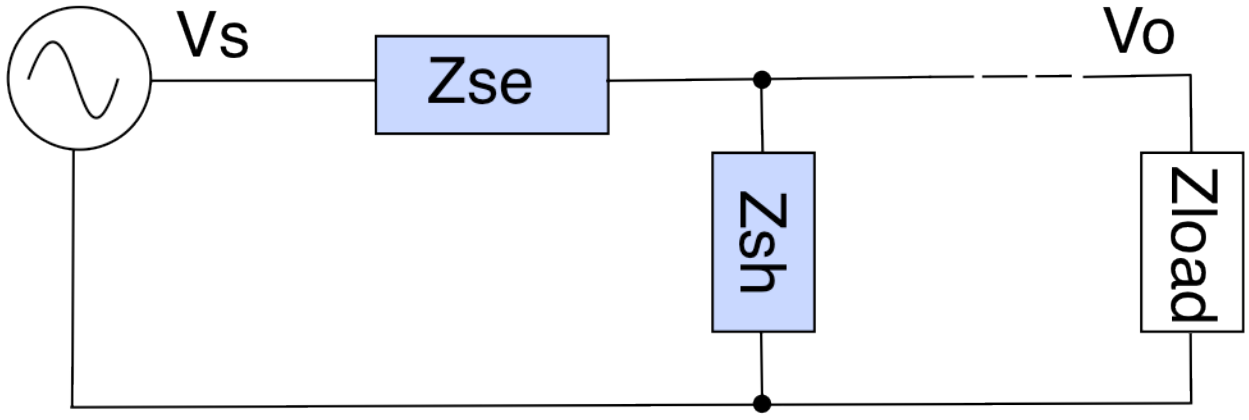
6 Common Layout Pitfalls…

1. Not Starting EMI Planning and Design Up Front
2. **Not Controlling EMI on *All* IO**

2. Control EMI on *All* IO

- Every signal entering or exiting must be shielded or filtered
- Shielded Cables – must connect connector shield to shield enclosure
- Unshielded cables (including shielded cables in a non-shielded enclosure)
- Need to keep common mode noise off cables
- Need to provide low RF impedance signal return paths – small loop areas

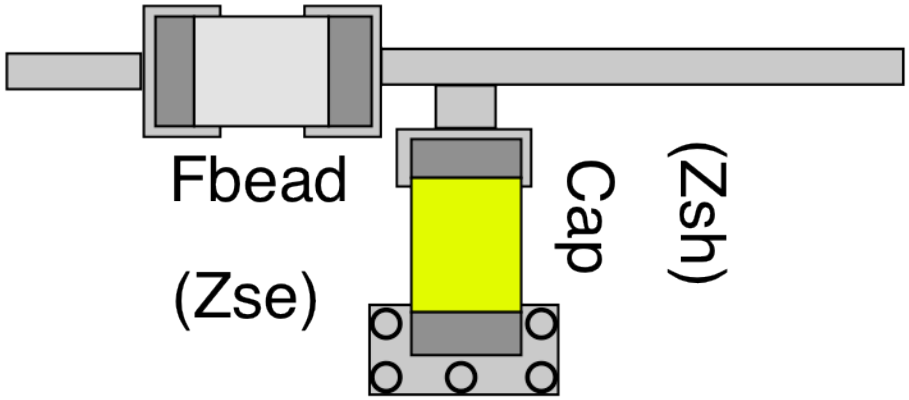
Filtering – Generally add Series Inductance or Resistance and Shunt Capacitance



$$\frac{Vo}{Vs} = \frac{Zsh \parallel Zload}{Zsh \parallel Zload + Zse} \approx \frac{Zsh}{Zse}$$

if Zload >> Zsh and
Zse >> Zsh

Example – add a series ferrite and a shunt capacitor



Typical Ferrite:
100 ohms at 100 MHz

Cap 0.001 uF:
1.6 ohms at 100 MHz

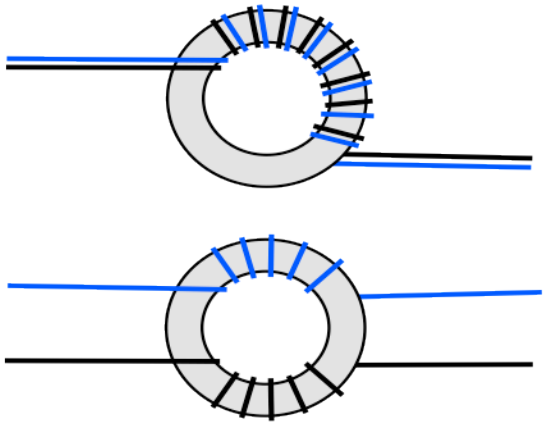
Attenuation ≈
1.6/100 - about 36 dB

(neglecting trace impedance and esr)

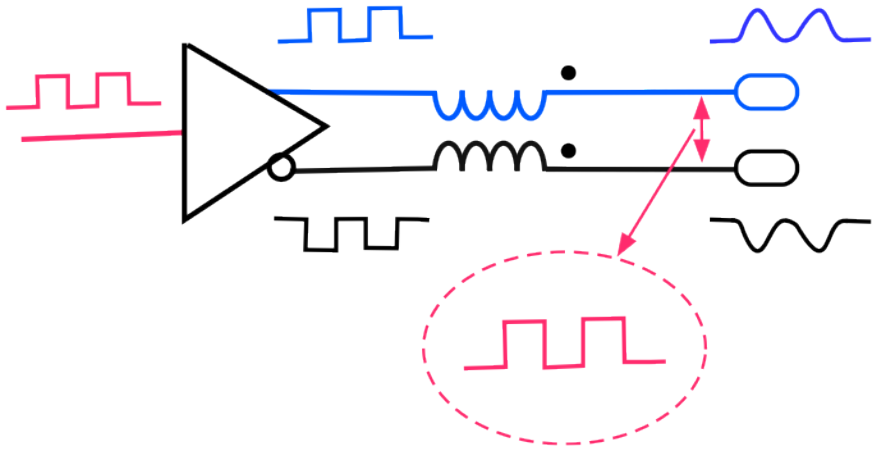
Some options for RF filtering IO

- Series Impedance
  - Ferrite or Resistor
- Shunt Cap to Ground reference
- Tee or Pi 3-terminal Filter, F-T Cap
- Common Mode Choke

Common Mode Chokes



- Two windings share magnetic field
- Fields cancel for Normal Mode – Low Z
- Fields add for Common Mode – High Z



- Differential (Normal) signal OK
- Common mode is blocked
- No Ground Needed

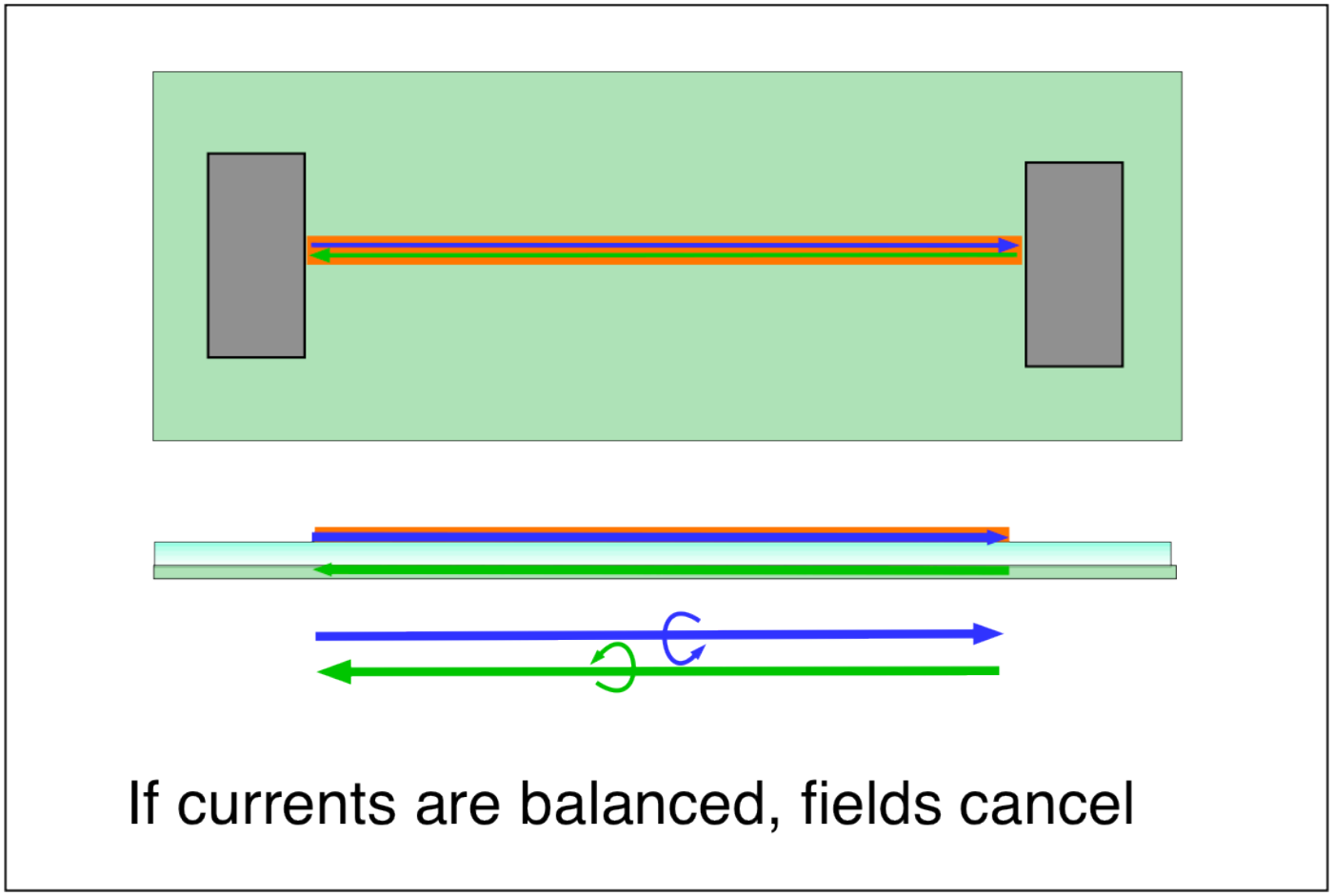
6 Common Layout Pitfalls…

1. Not Starting EMI Planning and Design Up Front
2. Not Controlling EMI on *All* IO
3. **Grounding / Return Discontinuities**

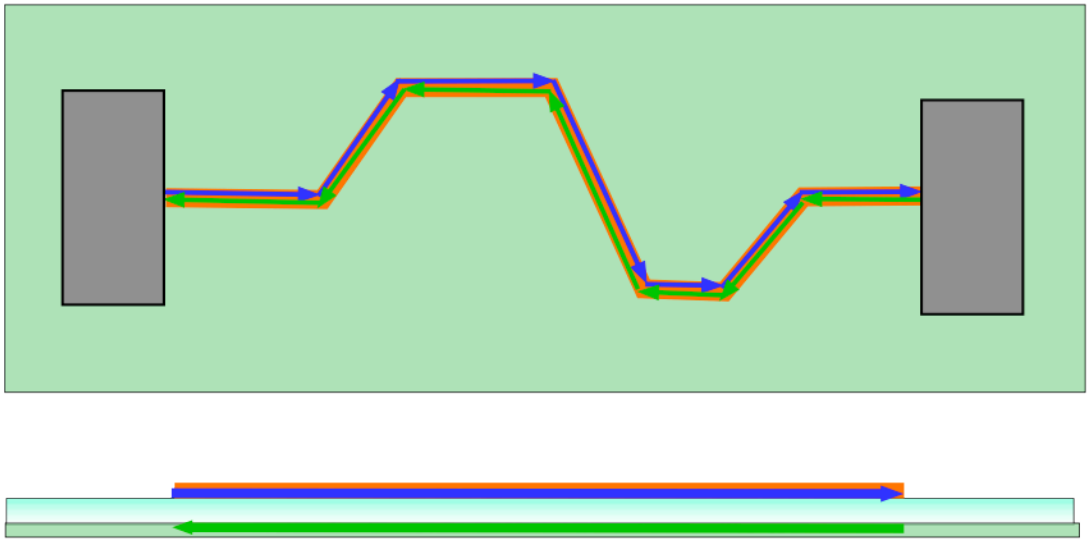
3. Traces routed over discontinuous ground plane

- Ground and planes are often misunderstood from RF/EMI perspective
- Classic "Single point grounding" usually is very bad for RF/EMI performance.
- Every trace over a ground plane is a **microstrip** line – so long as the ground plane is **continuous**.
- Traces routed over **gaps** in ground planes, power planes, and **via'd** from one plane to another (as in from a top to bottom layer) will cause EMI issues unless special provisions are made.

Trace over continuous ground plane – Microstrip – RF return current follows signal

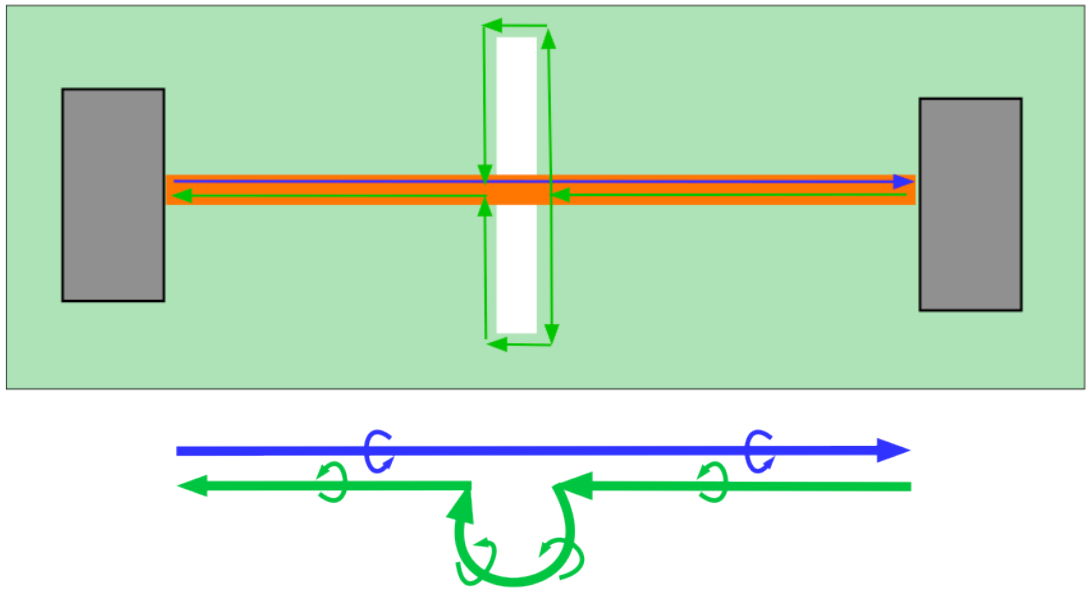


Trace over continuous ground plane – Microstrip – RF return current follows signal



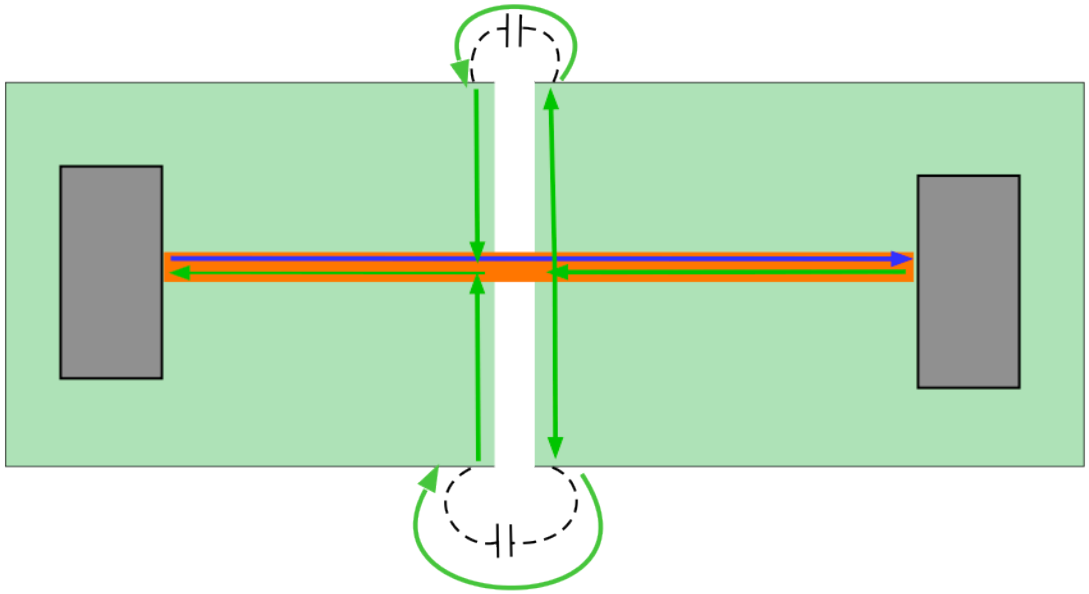
At RF Frequencies, the return current (in the ground plane) closely follows the signal path, so long as the ground plane is *continuous*.

Trace over discontinuous ground plane -- routing over gaps!



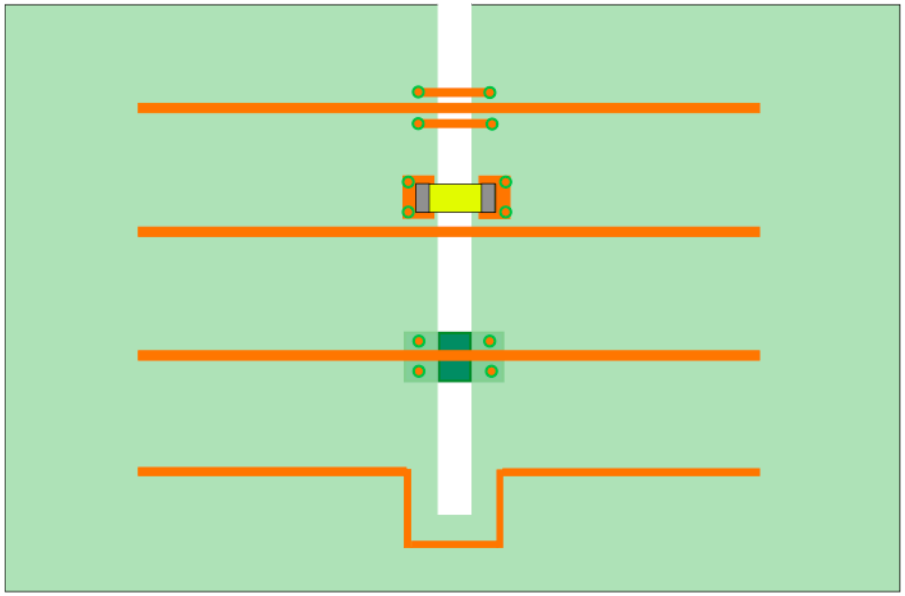
A large loop are is created, currents are no longer balanced, and a common mode current is introduced in the ground plane.

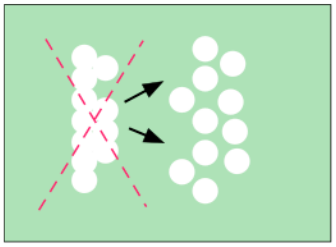
…Even worse with isolated planes



The return current **will** find a way back to the source, e.g., through stray capacitance. A significant antenna may be created.

Create a low impedance path for RF return currents

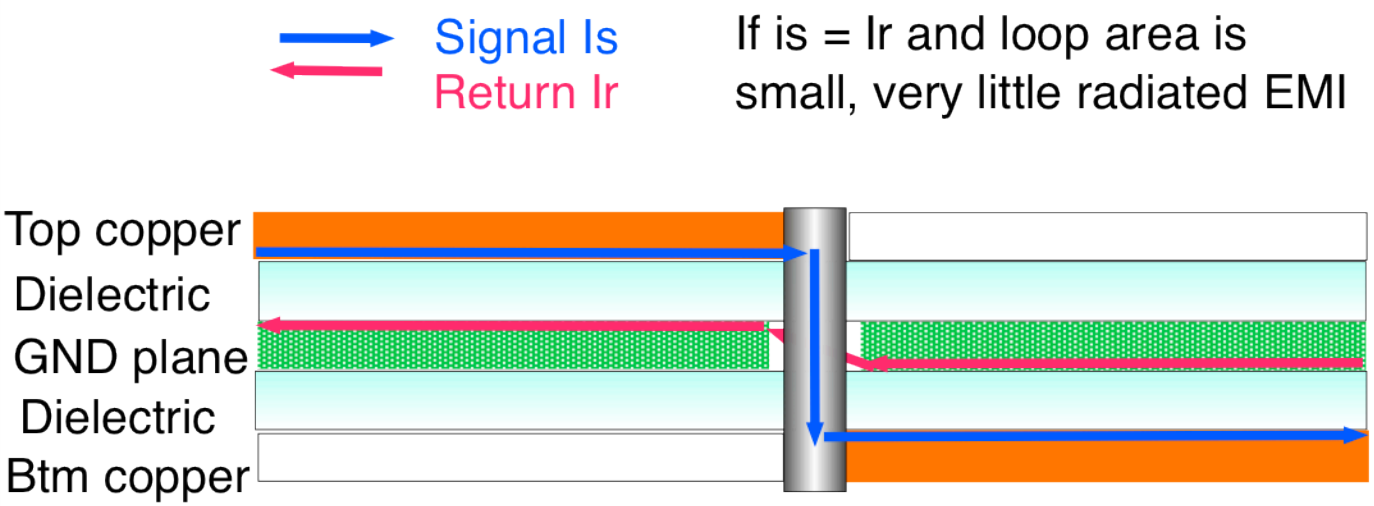




Watch for unintentional gaps in planes!

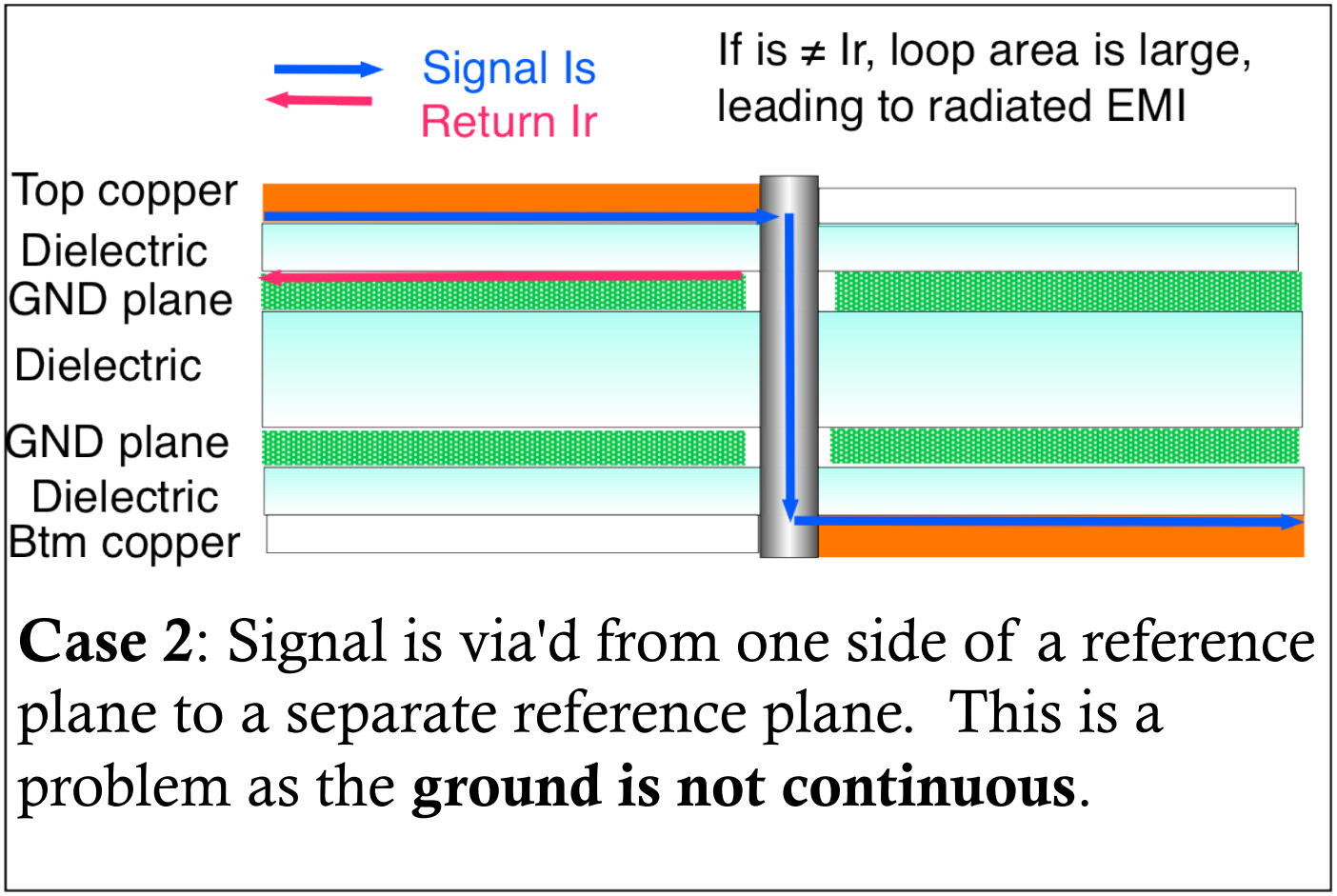
- Short “stitch” trace(s)
- RF Capacitor across gap
- Stitch to another plane
- Route around the gap

Changing Reference Planes



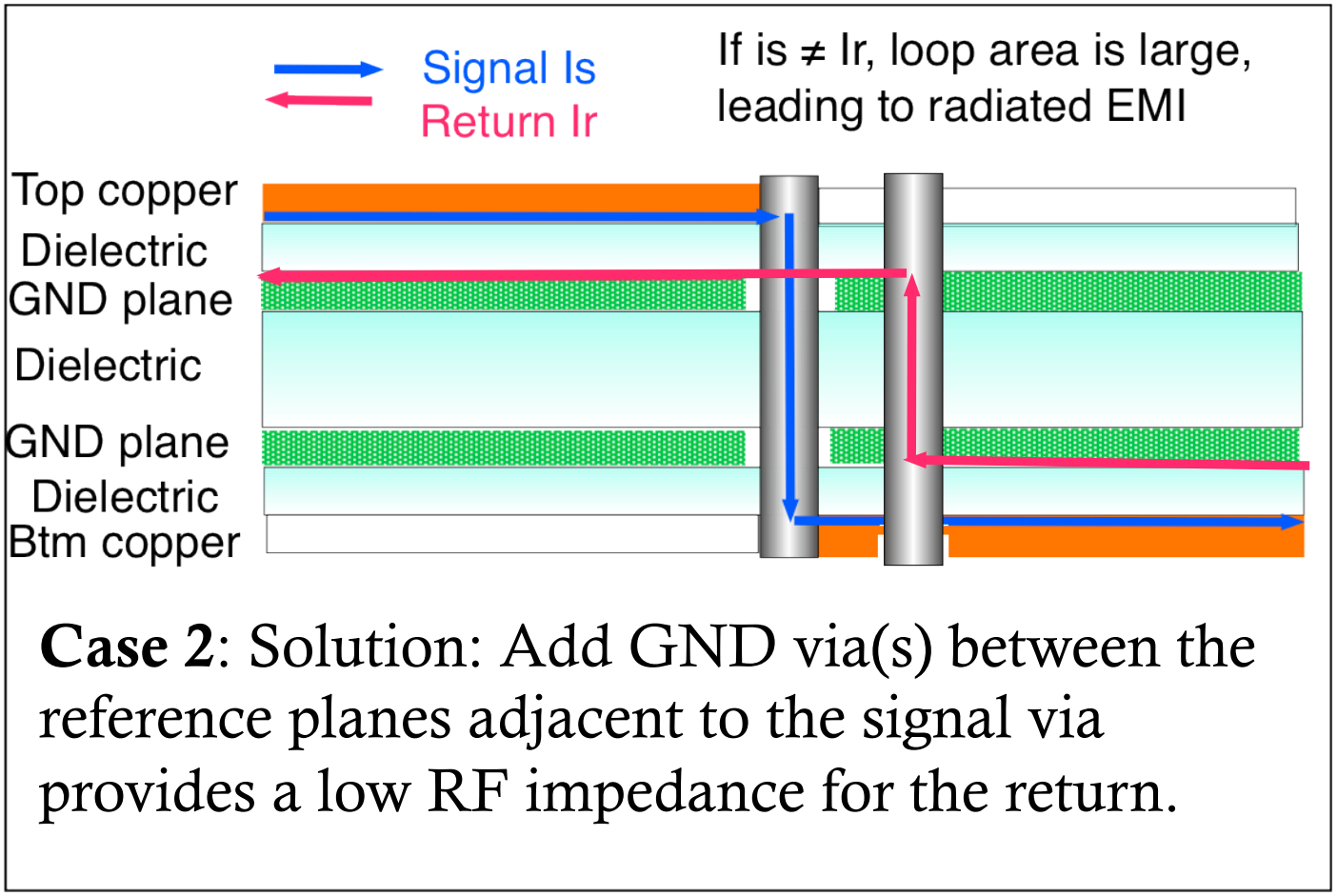
Case 1: Signal is via'd from one side of a reference plane to the other side of the
-- OK as the return path is continuous and can closely follow signal

Changing Reference Planes



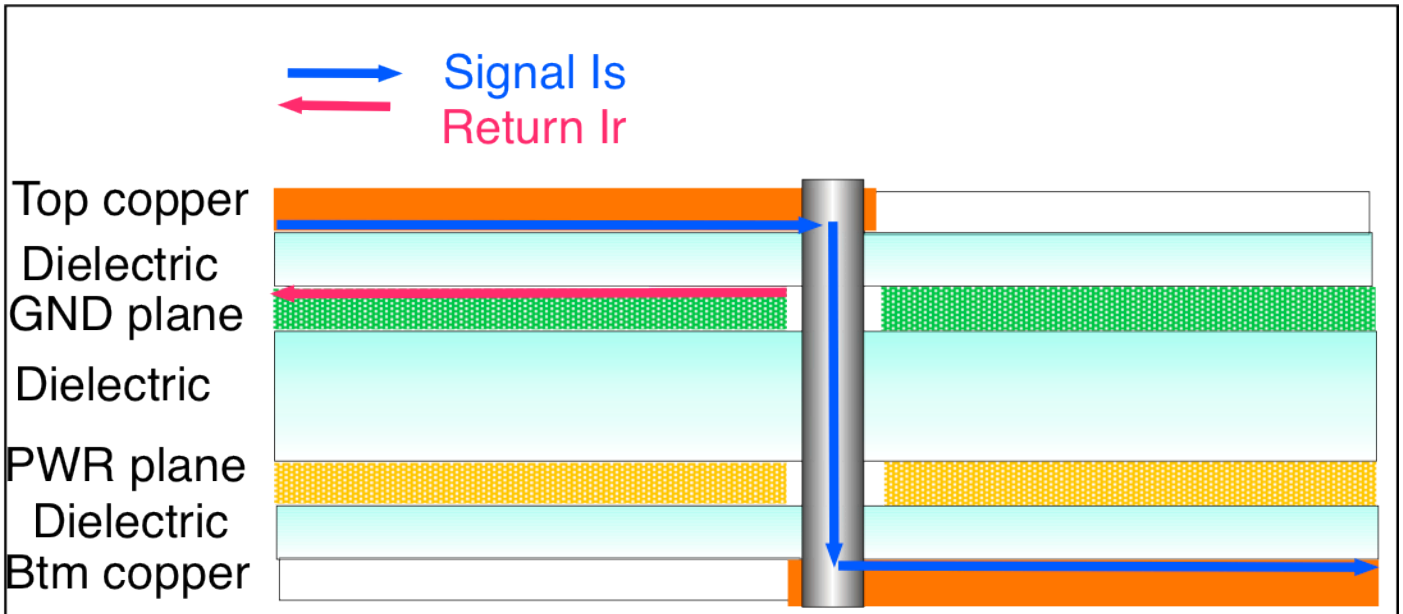
Case 2: Signal is via'd from one side of a reference plane to a separate reference plane. This is a problem as the **ground is not continuous**.

Changing Reference Planes



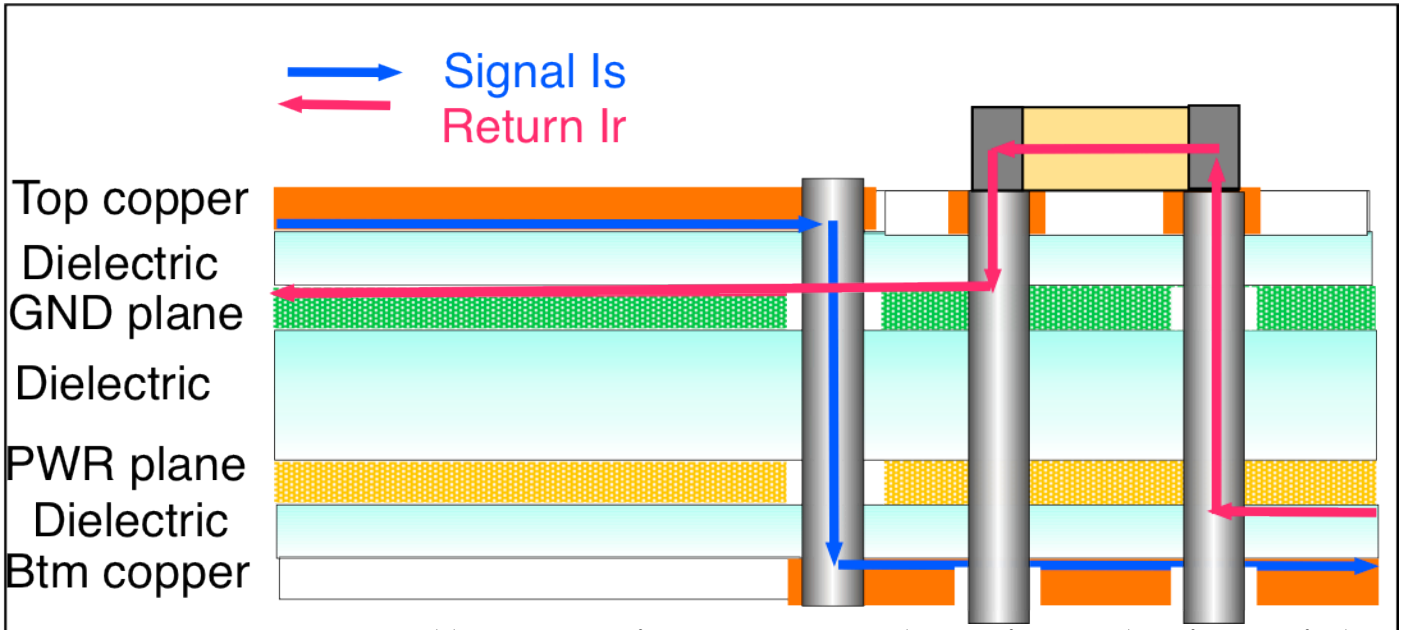
Case 2: Solution: Add GND via(s) between the reference planes adjacent to the signal via provides a low RF impedance for the return.

Isolated (e.g., power) Reference Planes



Case 3: Signal is via'd from a ground reference plane to an isolated (e.g., power) plane… No low impedance path for the RF return current.

Isolated (e.g., power) Reference Planes



Case 3: A small capacitor near the signal via with very low RF impedance to both planes (e.g., power and ground) provides a significantly improved return current path.

2-Layer Board Challenges

- Very difficult (or impossible) to route with an intact ground plane
- Large distance between plane and traces (e.g., 60 mils) reduces ground plane effectiveness
- Power distribution is problematic
- But, you **can** achieve acceptable EMI in many cases with care in design and layout

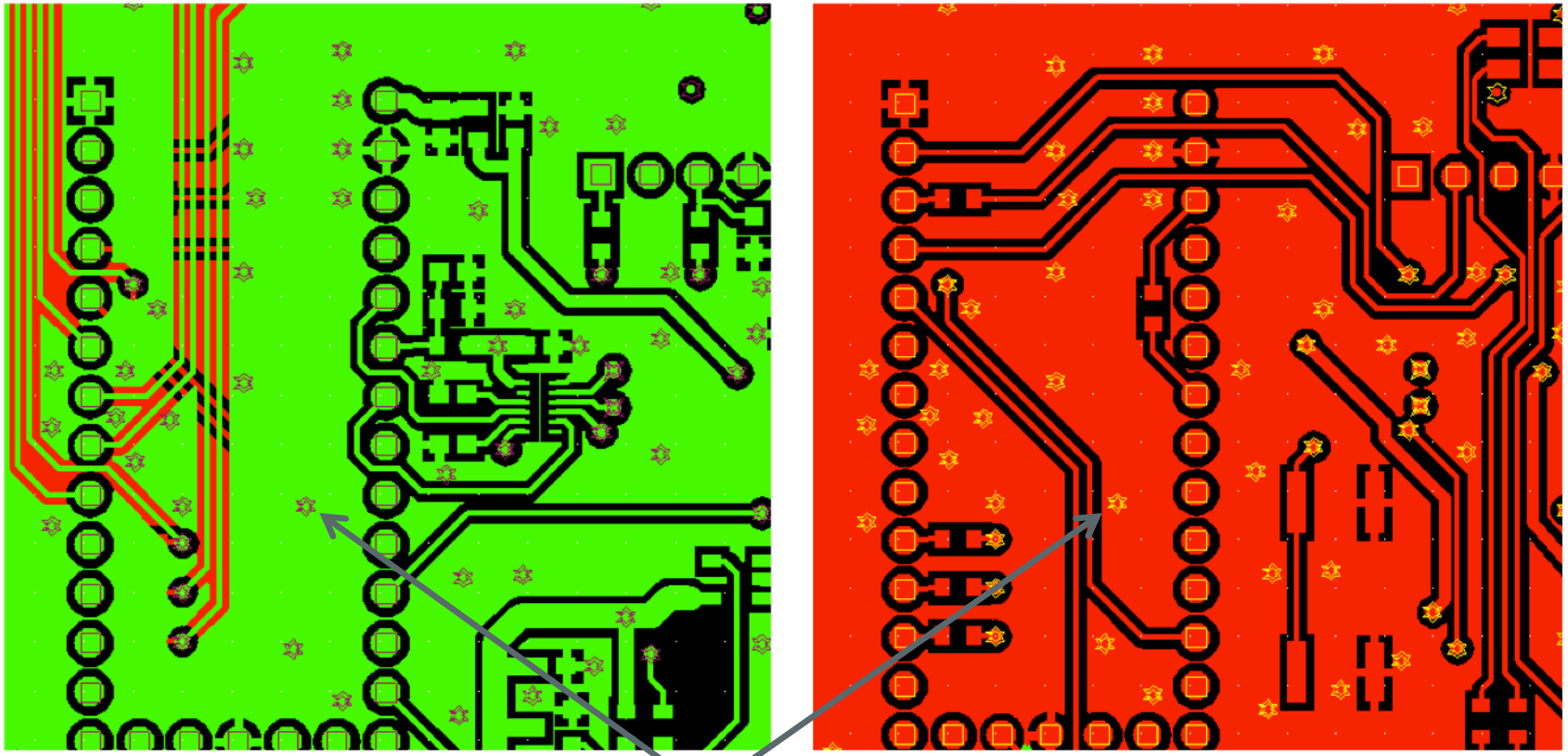
Some 2 Layer tips

- Keep any high speed areas very compact and don't run high speed IO traces around the board.
- Use LOTS of ground area. "Max fill" open space on both sides. Minimize and handle critical traces first with careful return current design.
- Route Power using wide traces and add a ferrite at the destination along with bypass caps on both side of the ferrite.

More 2 Layer tips

- Ground structure is 3D. Tie ground copper areas together with many stitch vias, short “ground tie” traces.
- Put impedance (ferrite or small resistor) in series with chips’ outputs to reduce peak current and dampen ringing.
- If a metal mounting structure is available, do tie the board ground structure to it across the board.
- If the board it too dense for these, use a 4 layer.

2 Layer Example – 2 radio modules, 72 MHz Micro, Switching PS



Top Side
Partial Detail

Stars show (GND) vias

Bottom Side
Partial Detail

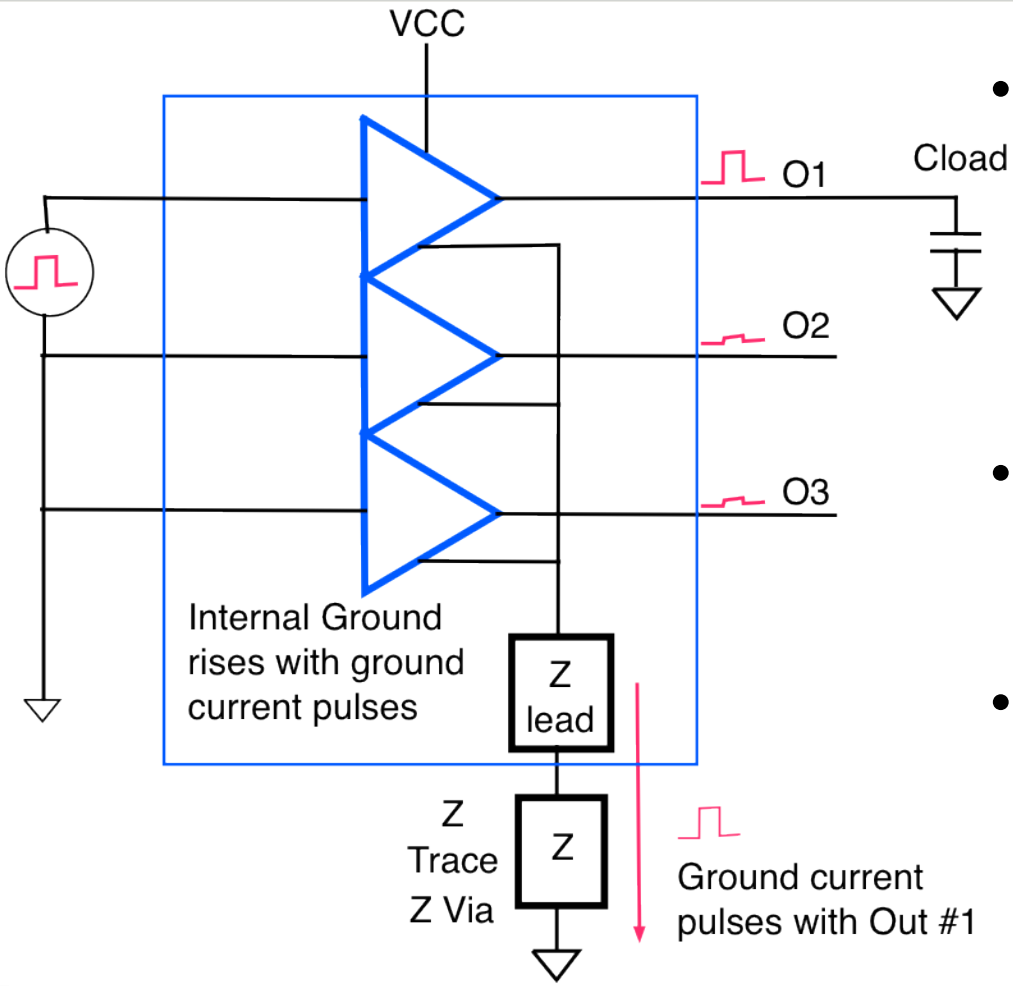
Summary: Avoiding the Discontinuous Ground Pitfall

- Use Ground Plane(s). If possible, **avoid gaps in it**.
- **Don't route across gaps in planes** or change reference planes without ensuring a **low RF impedance path at or near the via**.
- Most important for **high rise-time, high duty cycle**, but **all** signals can cause EMI!
- Route high speed traces and differential pairs **on a single layer if possible**.

6 Common Layout Pitfalls…

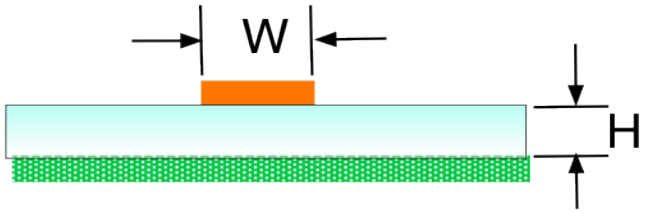
1. Not Starting EMI Planning and Design Up Front
2. Not Controlling EMI on *All* IO
3. Grounding / Return Discontinuities
4. **High Ground Impedance / Ground Bounce**

4. High Ground Impedance and Ground Bounce

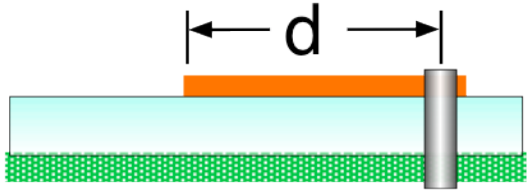


- Switching currents are coupled to other outputs through common impedance
- Low speed signals still can contain RF
- Must keep ground impedance low!

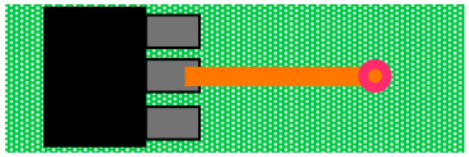
Trace and Via RF Impedance



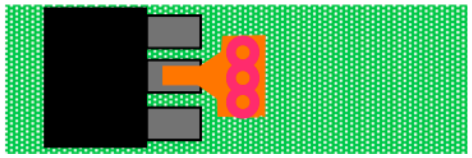
E.g, W=20 mils,
H=60mils; L≈16nH/in



A typical (16 mil) via
inductance L≈0.9 nH

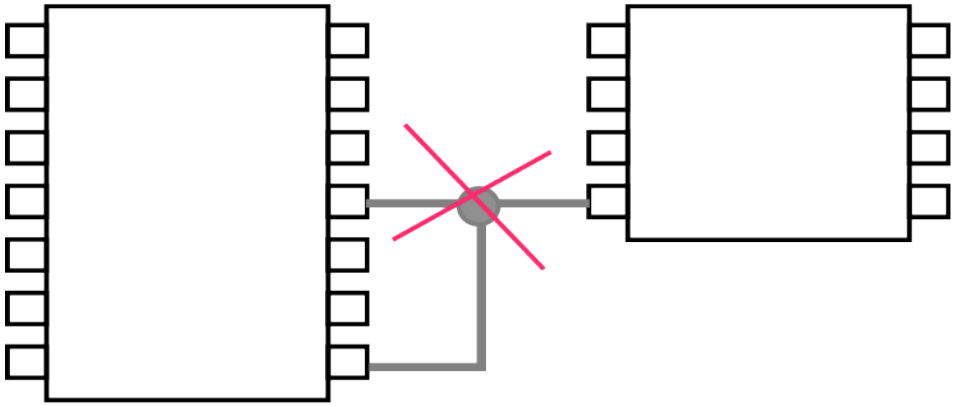


For a 3/4” trace and a
single via, L ≈13 nH
1t 100 MHz, XL ≈ 8 Ω

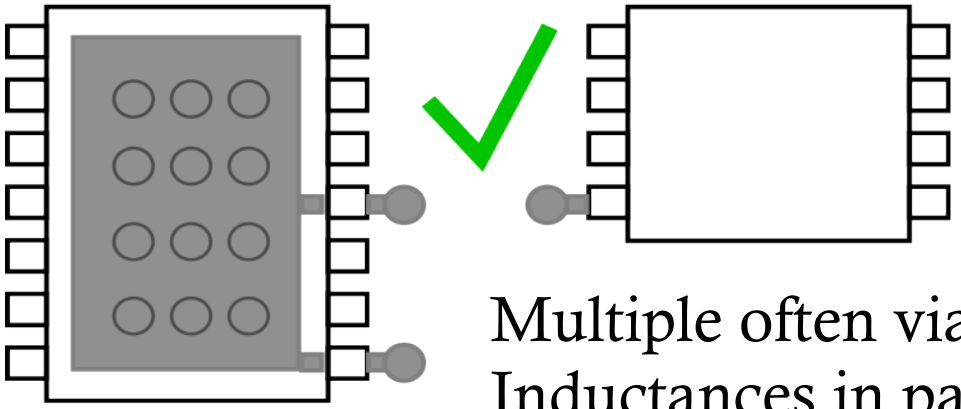


A very short, wide trace and
multiple vias could be 10X less!

Avoid this common error!



When layout personnel don't understand ground bounce



Route Grounds carefully and watch out for auto-routers!

Multiple often vias even better …
Inductances in parallel divide.

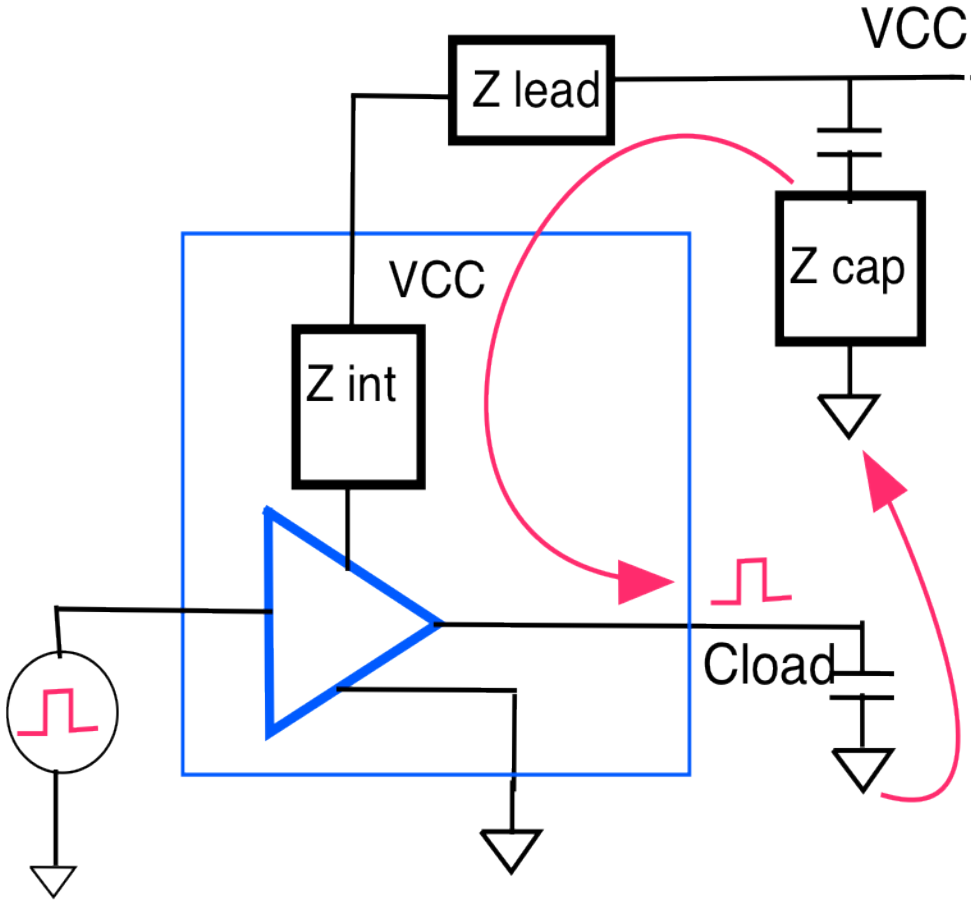
Summary: Avoiding Ground Bounce

- **Minimize Ground Inductance**
  - Never share ground vias or traces. In fact use multiples.
  - Keep ground traces short and fat (3:1)
  - Use a ground plane (even on a 2 layer board)
  - Use series impedance on IO to reduce peak current spikes.
  - Remember the *ALL* outputs are affected by ground bounce… not just the “fast” signals.

6 Common Layout Pitfalls…

1. Not Starting EMI Planning and Design Up Front
2. Not Controlling EMI on *All* IO
3. Grounding / Return Discontinuities
4. High Ground Impedance / Ground Bounce
5. **Poor Bypass and Power Distribution Design**

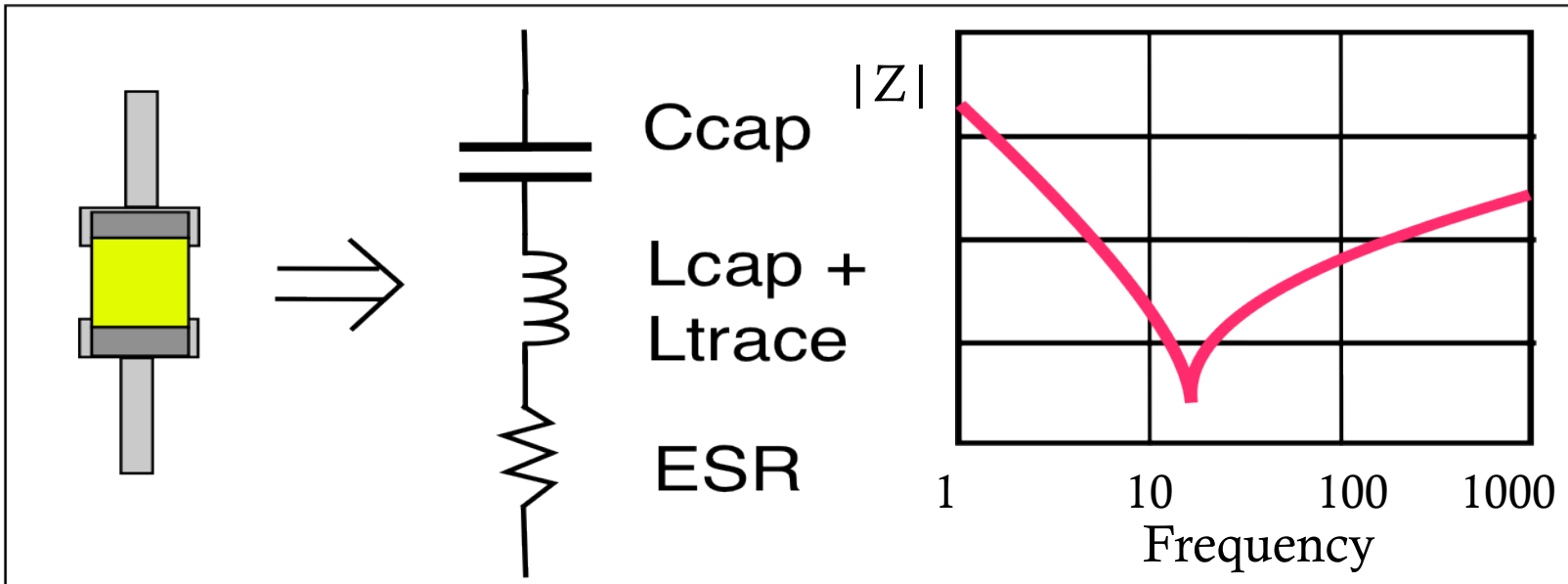
5. Poor Bypass and Power Distribution Design



Why Bypass?

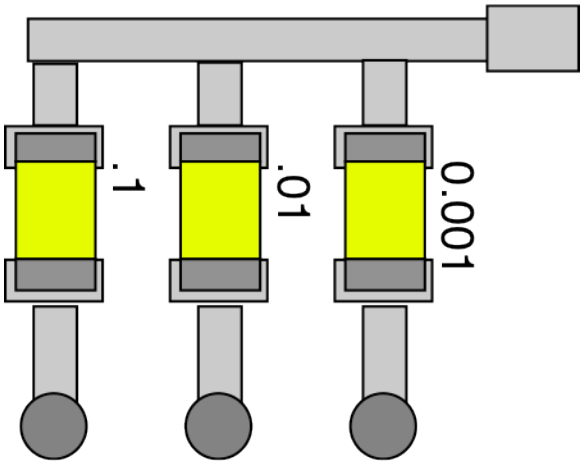
- Local HF caps provide the peak currents during switching
- Zcap, Zlead, and Zint must all be low at RF
- VCC bulk supply RF impedance is less important

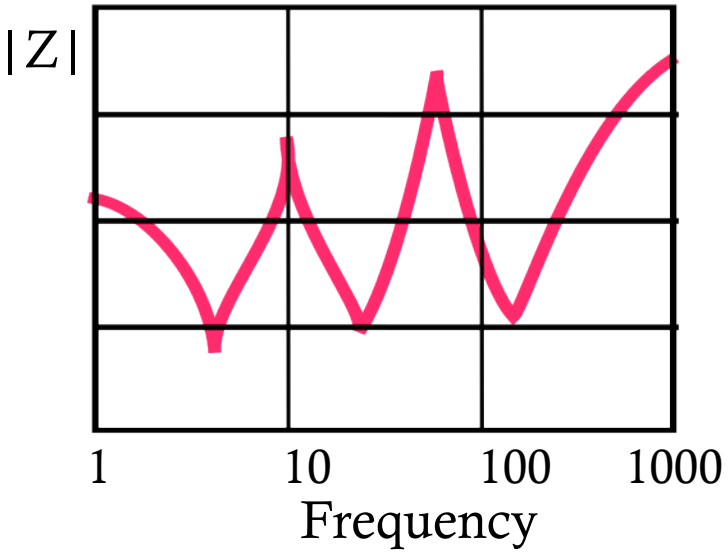
Simplified Real Component Model for SMT ceramic capacitors



Parasitic characteristics of capacitor and trace/ via. The graph shows a sample "self-resonance" where impedance rises after hitting a minimum.

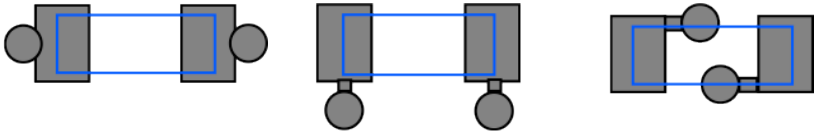
Multiple Capacitor Problem



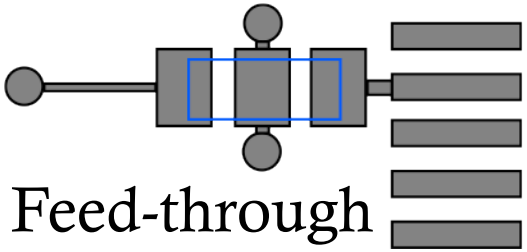


The concept is that each capacitor covers it own range. Often however, each capacitor and its routing contributes to both multiple series and parallel resonances which can be problematic.

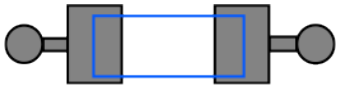
Bypass Layout for lower RF Impedance



Better



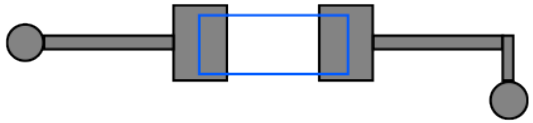
Feed-through Caps

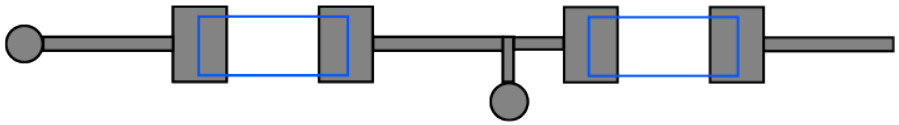


Poor

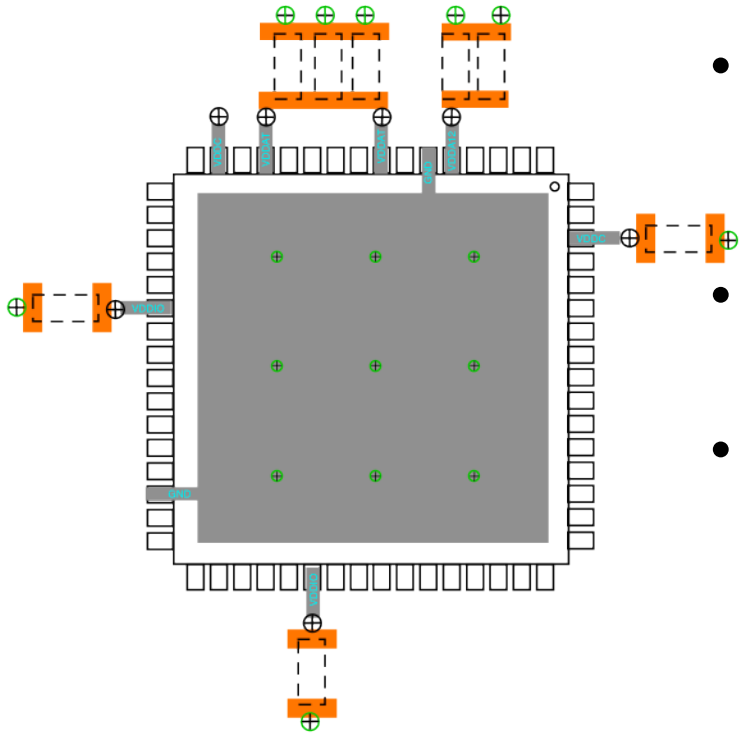
Note low-Z from power pin to cap and also from cap to GND

Terrible!





Practical chip example – Bypass caps on opposite side



(Based on a Reference Design)

- Ground area under chip and return GND pins to this.
- Stitch all ground vias to the continuous ground plane.
- Make a supplemental ground plane where practical on the bottom layer.
- Power fed from internal planes.

6 Common Layout Pitfalls…

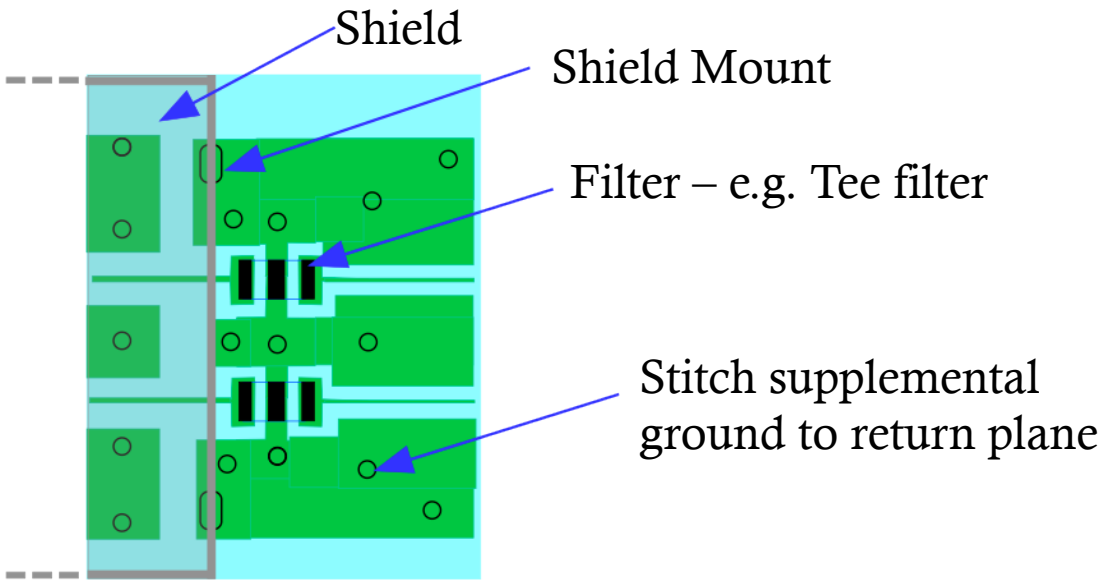
1. Not Starting EMI Planning and Design Up Front
2. Not Controlling EMI on *All* IO
3. Grounding / Return Discontinuities
4. High Ground Impedance / Ground Bounce
5. Poor Bypass and Power Distribution Design
6. **Contaminating "Clean" zones and Signals**

6. Don’t Contaminate your “clean” zones

- Don’t run a non-isolated (or unrelated) trace onto or across an isolated zone.
- In most cases, an isolated zone (e.g., opto or transformer isolated) should be isolated on all layers.
- Don’t route a cable over the PCB. Near field coupling can be very efficient at contaminating the cable!
- Don’t run an unbalanced high current, high di/dt signal through the ground plane. Use a separate low RF impedance path. Example – Switching supplies.

6. Don’t Contaminate your “clean” zones

- Zone your board carefully… keep noisy areas confined with minimum high speed interconnections
- Consider using board level shield(s)

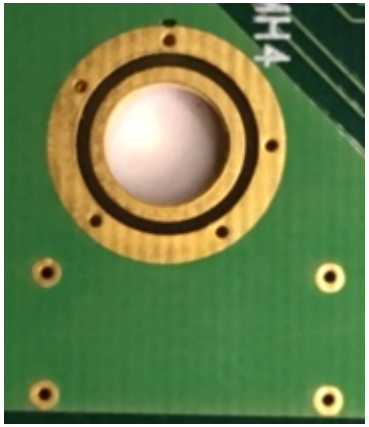


Tips for Debug and Test

- Plan some options in layout at first prototype. You can take them out later to save cost.
- …Add pads for enough caps to allow isolated ground areas to be tied down at RF if needed.
- …add pads for an R-C damper/snubber on switching supplies to reduce ringing if detected.
- …add pads for resistors across the inductor in LC filters to add damping if needed.
- Leave some ground pads /vias uncovered for probing.

Tips for Debug and Test

- Keep a board or two out of conformal coat for testing… Very hard to test and modify after conformal coat.
- Consider mounting hole designs to allow plane to be tied to metal mounting in different ways for best EMI performance.

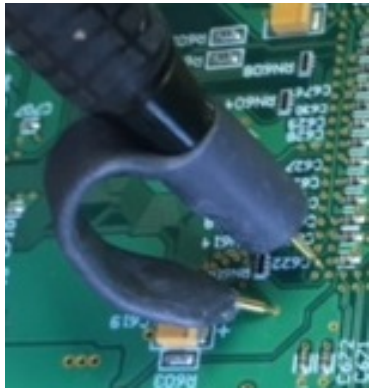


- Options for connecting planes to enclosure
- Can provide pads for Caps and inductors as well

Tips for Debug and Test

- Plan for probing the board after fabrication…

Low-Z probe with
very short ground lead



Near-field H field Probe
and RF Current Probe

Summing up…

- Plan for good EMC performance up front.
- Use the lowest rise times, shortest signal paths, lowest RF currents practical for critical signals.
- Remember inductance dominates at RF.
- Pay close attention to return currents and return current paths. Don't unbalance balances lines.
- Group (if possible) and Filter all IO

Questions?

Thank You!

Stop by the ESDI table for more Info

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